

HS6220 2.4G Register Map

Version 1.1

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Revision History

Revision	Date	Description
V0.1	Nov 14, 2019	Initial Draft
V0.2	Feb 18, 2020	Update some register
V0.3	Mar 6, 2020	Add CAL_DONE in RF_SETUP CTUNING and FTUNING change to 6200 Add software instruction for vco_amp_tx_mux
V0.4	Mar 10, 2020	Remove test_pat reg Add ble_crc_init reg Add ble_timer reg Add xn_en reg
V0.5	Mar 17, 2020	Add RF_DOMAIN_EN in PMU_CTL reg
V0.6	Mar 19, 2020	Add RF_PWRDWN Remove RF_DOMAIN_EN Remove DIGLDO_EN Remove RF_RSTN Remove RF_ISO_EN Remove RF_GATE_EN Remove Tx_wait_cnt
V0.7	Mar 26, 2020	Add miso_drv Add bypass_io Add reg_output_en and reg_output
V0.8	May 13, 2020	Add registers for BLE mode
V0.9	May 14, 2020	Default value of PRIM_RX is changed to 1
V1.0	May 29, 2020	Move scramble_en from register CAL_CTL to register EN_RXADDR
V1.1	Jul 5, 2020	Remove BLE register

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Register Definition

BANK0

CONFIG (RW) Address: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_gurd_en	MASK_RX_DR	MASK_TX_DS	MASK_MAX_RT	EN_CRC	CE_REG	PWR_UP	PRIM_RX
1	0	0	0	1	0	0	1
RW	RW	RW	W	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7	1	Tx_gurd_en	Bypass tx guard enable
6	0	MASK_RX_DR	Mask interrupt caused by RX_DR
			0 Reflect RX_DR as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
5	0	MASK_TX_DS	Mask interrupt caused by TX_DS
			0 Reflect TX_DS as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
4	0	MASK_MAX_RT	Mask interrupt caused by MAX_RT
			0 Reflect MAX_RT as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
3	1	EN_CRC	Enable CRC. Forced high if one of the bits in the EN_AA is high
			0 Disable CRC
			1 Enable CRC
2	0	CE_REG	CE controlled by register
			0
			1
1	0	PWR_UP	Power up control
			0 POWER DOWN
			1 POWER UP
0	1	PRIM_RX	RX/TX control
			0 PTX
			1 PRX

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EN_AA (RW) Address: 01h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed					ENAA_P2	ENAA_P1	ENAA_P0
0					1	1	1
RW					RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7:3	0	Reserved	
2	1	ENAA_P2	Enable auto acknowledgement data pipe 2
			0 Disable
			1 Enable
1	1	ENAA_P1	Enable auto acknowledgement data pipe 1
			0 Disable
			1 Enable
0	1	ENAA_P0	Enable auto acknowledgement data pipe 0
			0 Disable
			1 Enable

EN_RXADDR (RW) Address: 02h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed				scramble_en	ERX_P2	ERX_P1	ERX_P0
0				1	0	1	1
RW				RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7:4	0	Reserved	
3	1	scramble_en	Scramble enable
			0 Disable
			1 Enable
2	0	ERX_P2	Enable data pipe 2
			0 Disable
			1 Enable
1	1	ERX_P1	Enable data pipe 1
			0 Disable

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			1	Enable
0	1	ERX_P0	Enable data pipe 0	
			0	Disable
			1	Enable

PMU_CTL (RW) Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rtc32k_rdy_enb_reg	Rtc32k_rdy_enb_mn	Digldo_enb_dly_reg	Digldo_enb_mn	Digldo_enb_reg	rtc32k_en	RF_PWRDWN[1:0]	
1	0	1	0	1	0	01	
RW	RW	RW	RW	RW	RW	RW	

Description of Word

Bit	Value	Symbol	Description
7	1	Rtc32k_rdy_enb_reg	For debug mode
6	0	Rtc32k_rdy_enb_mn	Rtc32k manual mode select, 0 for fsm control; 1 for manual mode
5	1	Digldo_enb_dly_reg	For debug mode
4	0	Digldo_enb_mn	Digital ldo manual mode select, 0 for fsm control; 1 for manual mode
3	1	Digldo_enb_reg	For debug mode
2	0	rtc32k_en	Rtc32k enable, 0 for disable; 1 for enable
1:0	2'b01	RF_PWRDWN[1:0]	Working mode select 00 active mode 01 deep sleep mode 10 light sleep mode

SETUP_RETR (RW) Address: 04h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ARD				ARC			
4'b0				4'b11			
RW				RW			

Description of Word

Bit	Value	Symbol	Description
7:4	4'b0	ARD	Auto Retransmit Delay

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			4'hf	Wait 4000 μ S
		
			4'h1	Wait 500 μ S
			4'h0	Wait 250 μ S
3:0	4'b11	ARC	Auto Retransmit Count	
			4'hf	Up to 15 Re-Transmit on fail of AA
		
			4'h1	Up to 1 Re-Transmit on fail of AA
			4'h0	Re-Transmit disabled

RF_CH (RW) Address: 05h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_Rf_ch							
0x32							
RW							

Description of Word

Bit	Value	Symbol	Description
8:0	2	Reg_Rf_ch	Sets the frequency channel HS6200 operates on

RF_SETUP (RW) Address: 06h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONT_WAVE	PA_PWR[3]	CAL_DONE	CAL_EN	RF_DR_HIGH	Pa_power		
0	1	0	1	0	3'b000		
RW	RW	RW	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description
7	0	CONT_WAVE	Enables continuous carrier transmit when high
			0 Disable
			1 Enable
6	1	PA_PWR[3]	PA power select bit 3
5	0	CAL_DONE	Flag for calibration finishing, after CAL_EN set to 1, CAL_DONE will be reset to 0 0 calibration on 1 calibration done

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4	0	CAL_EN	Calibration enable, 1 for enable; 0 for disable		
3	1	RF_DR_HIGH	Data rate select, 1 for 2Mbps; 0 for 1Mbps		
2:0	3'b010	PA_PWR[2:0]	PA power control, PA_PWR[3:0] with pa_voltage of RF_IVGEN in bank1		
			PA_PWR[3:0]	Pa_voltage(bank1 of RF_IVGEN)	
			1111	0	Output 8 dbm,
			1000	0	Output 5 dbm
			0111	1	Output 4dbm,
			0011	0	Output 0 dbm,
			0001	0	Output -6 dbm
			0001	1	Output -12 dbm
			0000	0	Output -16 dbm
			0000	1	Output -43 dbm

STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	SYNC_DS	CE	RX_P_NO		TX_FULL
0	0	0	0	0	2'b11		0
R	RW	RW	RW	R	R		R

Description of Word

Bit	Value	Symbol	Description	
7	0	BANK	Register BANK status	
			1	Register R/W is to register BANK1
			0	Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.	
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. Write 1 to clear bit.	
4	0	SYNC_DS	RX sync detector interrupt, Write 1 to clear bit. If SYNC_DS is asserted it must be cleared to enable further communication.	
3	0	CE	CE state	
2:1	2'b11	RX_P_NO	Data pipe number for the payload available for reading from RX_FIFO	
			11	RX FIFO Empty
			00-10	Data Pipe Number
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

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RX_ADDR_P0 (RW) Address: 0Ah

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
RX_ADDR_P0							
8'h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
RX_ADDR_P0							
8'h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RX_ADDR_P0							
8'h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RX_ADDR_P0							
8'h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P0							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
39:0	40'7041 882046	RX_ADDR_P0	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)

RX_ADDR_P1 (RW) Address: 0Bh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P1							
8'hC2							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc2	RX_ADDR_P1	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

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RX_ADDR_P2 (RW) Address: 0Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P2							
8'hC3							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc3	RX_ADDR_P2	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

TX_ADDR(RW) Address: 10h

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
TX_ADDR							
8'h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
TX_ADDR							
8'h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
TX_ADDR							
8'h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TX_ADDR							
8'h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_ADDR							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
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39:0	40'h704 1882046	TX_ADDR	Transmit address. Used for a PTX device only. (LSByte is written first)Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Protocol engine enabled.
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RX_PW_P0 (RW) Address: 11h

The register has two definition for 2.4G mode and 2.4G long packet mode respectively

2.4G mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P0					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description
7:6	2'b00	Reserved	
5:0	6'h00	RX_PW_P0	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes)
			32 32 bytes
			...
			1 1 byte
			0 Pipe not used

2.4G long packet mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Long_packet_legth_p0[7:0]							
0							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'h00	Long_packet_length_p0	Payload length of 2.4G long packet mode, 0~255

RX_PW_P1 (RW) Address: 12h

The register has two definition for 2.4G mode and 2.4G long packet mode respectively

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2.4G mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P1					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description
7:6	2'b00	Reserved	
5:0	6'h00	RX_PW_P1	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes)
			32 32 bytes
		
			1 1 byte
			0 Pipe not used

2.4G long packet mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Long_packet_legh_p1[7:0]							
0							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'h00	Long_packet_length_p1	Payload length of 2.4G long packet mode, 0~255

RX_PW_P2 (RW) Address: 13h

The register has two definition for 2.4G mode and 2.4G long packet mode respectively

2.4G mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P2					
0		0					
RW		RW					

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Description of Word

Bit	Value	Symbol	Description
7:6	2'b00	Reserved	
5:0	6'h00	RX_PW_P2	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes)
			32 32 bytes
		
			1 1 byte
			0 Pipe not used

2.4G long packet mode:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Long_packet_legth_p2[7:0]							
0							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'h00	Long_packet_length_p2	Payload length of 2.4G long packet mode, 0~255

FIFO_STATUS (RW) Address: 17h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TX_REUSE_PL	TX_FULL	TX_EMPTY	Reserved		RX_FULL	RX_EMPTY
0	0	0	1	0		0	1
RW	R	R	R	RW		R	R

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	Only '0' allowed
6	0	TX_REUSE_PL	0 Keep the current value
			1 Reset to default values
			TX REUSE flag.
5	0	TX_FULL	1 Tx data reused
			0 Tx data not reused
			TX FIFO full flag.

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			1	TX FIFO full
			0	Available locations in TX FIFO
4	1	TX_EMPTY	TX FIFO empty flag.	
			1	TX FIFO empty
			0	Data in TX FIFO
3:2	2'b00	Reserved	Only '00' allowed	
			0	Keep the current value
			1	Reset to default values
1	0	RX_FULL	RX FIFO full flag.	
			1	RX FIFO full
			0	Available locations in RX FIFO
0	1	RX_EMPTY	RX FIFO empty flag.	
			1	RX FIFO empty
			0	Data in RX FIFO

CONFIG_EXT (RW) Address: 18h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				msk_rx_afull	msk_tx_aempty	Reserved	
4'h1				1	1	2'b10	
RW				RW	RW	RW	

Description of Word

Bit	Value	Symbol	Description
7:4	4'h1	Reserved	
3	1	msk_rx_afull	
2	1	msk_tx_aempty	
1:0	2'b10	Reserved	

DYNPD (RW) Address: 1Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_output	Reg_output_en	Bypass_io	Xn_en	Spi4_en	DPL_P2	DPL_P1	DPL_P0
0	0	1	0	0	0	0	0
RW		RW	RW	RW	RW	RW	RW

Description of Word

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Bit	Value	Symbol	Description
7	0	Reg_output	Register control IRQ output
6	0	Reg_output_en	Register control IRQ output enable
5	1	Bypass_io	Bypass IRQ and MOSI, after HS6220 power up, Bypass_io should be set 0
4	0	Xn_en	Xn mode enable
3	0	Spi4_en	4-wire SPI enable
2	0	DPL_P2	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
1	0	DPL_P1	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
0	0	DPL_P0	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)

FEATURE (RW) Address: 1Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Long_packet_en	Ble_en	Soft_rst	BP_GAU	Vco_amp_tx_mux	EN_DPL	EN_ACK_PAY	EN_DYN_ACK
0	0	0	1	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7	0	Long_packet_en	Long packet mode enable
6	0	Ble_en	BLE mode enable
5	0	Soft_rst	Software reset
4	1	BP_GAU	Bypass Gaussian filter, BLE mode should not bypass Gaussian filter
3	1	Vco_amp_tx_mux	Vco_amp_tx_mux=0, vco_amp_ctr[3:0] (VCO amplitude control bit) of RX and TX are both from calibration fsm; Vco_amp_tx_mux=1, vco_amp_ctr[3:0] of RX is from calibration fsm, vco_amp_ctr[3:0] of TX is fixed to 0x0c;
2	0	EN_DPL	Enables Dynamic Payload Length
1	0	EN_ACK_PAY	Enables Payload with ACK
0	0	EN_DYN_ACK	Enables the W_TX_PAYLOAD_NOACK command

SETUP_VALUE (RW) Address: 1Eh

Bit23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit17	Bit16
REG_LNA_WAIT							
8'h00							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit8
REG_MBG_WAIT							

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8'h06							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_TM_CNT							
8'h80							
RW							

Description of Word

Bit	Value	Symbol	Description	
23:16	8'h00	REG_LNA_WA IT	Lna wait counter	
			8'hff	255 cycle
		
			1	1 cycle
			0	0 cycle
15:8	8'h06	REG_MBG_W AIT	Main bandgap wait counter	
			8'hff	255us
		
			1	1 us
			0	0 us
7:0	8'h80	RX_TM_CNT	Rx timeout counter.	
			8'hff	255us
		
			1	1 us
			0	0 us

PRE_GURD (RW) Address: 1Fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPARE_REG[7:0]							
0							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAIL_CTL			GRD_EN	GRD_CNT			
011			1	4'h7			
RW			RW	RW			

Description of Word

Bit	Value	Symbol	Description
15:8	0	SPARE_REG	Reserved register

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7:5	3'h3	TAIL_CTL	Number of repeat bit after the CRC	
			7	7 repeat tail
		
			1	1 repeat tail
			0	0 No repeat tail
4	1	GRD_EN	Pre-Guard enable	
3:0	4'h7	GRD_CNT	Number of Pre-Guard bit before preamble	
			4'hf	16 bit pre_guard
		
			1	2 bit pre_guard
			0	1 bit pre_guard

BANK1

LINE (R) Address: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CID							
8'h06							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CID							
8'h00							
R							

Description of Word

Bit	Value	Symbol	Description
15:0	16'h060 0	CID	Chip ID

PLL_CTL0 (RW) Address: 01h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
SDM_EN	PLL_dac_en	PLL_RSTN_ PFD	CRY_PD_RE G	CRY_PD_M N	Reserved	PLL_FOFFSET_SEL	
1	1	1	0	0	0	01	

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RW	RW	RW	RW	RW	RW	RW	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
DAC_CAL_E N_REG	DAC_CAL_ EN_MN	DAC_CALM ODE_REG	BP_RC_BP	DOC_CAL_ EN_REG	DOC_CAL_ EN_MN_	DOC_DAC_ MN	I_Q_RVS
0	0	0	1	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PLL_TEST_ EN	pd_pkdet_reg	pd_pkdet_mn	PD_PLL_RE G	PD_PLL_M N	PLL_TX_EN _REG	PLL_TX_EN _MN	BYPASS_VC O_RES
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDM_DITH_ IN	SDM_DITH_ EN	DAC_RANG E_MN	SYNC_DET_ DIS	AFC_EN_RE G	AFC_EN_M N	CTUNING_ MN	FTUNING_ MN
0	1	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
31	1	SDM_EN	SDM enable	
			1	Enable the SDM
			0	Disable the SDM
30	1	Pll_dac_en	Output DAC_EN to analog	
			0	Output 0
			1	Output 1
29	1	PLL_RSTN_PFD D	PLL_RSTN_PFD control	
			1	Set 1
			0	Set 0
28	0	CRY_PD_REG	Control the Power down of Crystal	
			1	Power down the crystal
			0	Power up the crystal
27	0	CRY_PD_MN	Select the source of crystal power down	
			1	CRY_PD = CRY_PD_REG
			0	CRY_PD = CRY_PD_FSM
26	0	Reserved		
25:24	01	PLL_FOFFSET _SEL	PLL_FOFFSET_SEL control	
23	0	DAC_CAL_EN _REG	DAC calibration enable	
			1	Enable the DAC calibration
			0	Disable the DAC calibration

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22	0	DAC_CAL_EN_MN	Select the source of DAC_CAL_EN	
			1	DAC_CAL_EN = DAC_CAL_REG
			0	DAC_CAL_EN = DAC_CAL_FSM
21	0	DAC_CALMO_DE_REG	Control the VCO gain	
			1	Normal gain
			0	5 times of the normal gain
20	1	BP_RC_BP	Bypass RC_BP phase in the FSM	
			1	Bypass RC_BP phase
			0	No bypass RC_BP phase
19	0	DOC_CAL_EN_REG	Enable the DOC calibration	
			1	Enable the DOC calibration
			0	Disable the DOC calibration
18	0	DOC_CAL_EN_MN	Select the source of DOC_CAL_EN source	
			1	DOC_CAL_EN = DOC_CAL_EN_REG
			0	DOC_CAL_EN = DOC_CAL_EN_FSM
17	0	DOC_DAC_MN	Select the source of DOC source	
			1	DOC_DACI = DOC_DACI_REG DOC_DACQ = DOC_DACQ_REG
			0	DOC_DACI = DOC_DACI_FSM DOC_DACQ = DOC_DACQ_FSM
16	0	I_q_rvs	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
15	0	PLL_TEST_EN	Enable the PLL in test mode	
			1	PLL A_CNT and B_CNT come from register
			0	PLL A_CNT and B_CNT come from SDM
14	0	pd_pkdet_reg	Manual mode of pd_pkdet register	
13	0	pd_pkdet_mn	Manual mode of pd_pkdet enable	
12	0	PD_PLL_REG	PLL power down control	
			1	Power down PLL
			0	Power up PLL
11	0	PD_PLL_MN	Select the source of PLL Power down	
			1	PD_PLL = PD_PLL_REG
			0	PD_PLL = PD_PLL_FSM
10	0	PLL_TX_EN_REG	PLL TX mode	
			1	PLL in TX mode
			0	PLL in RX mode
9	0	PLL_TX_EN_MN	Select the source of PLL_TX_EN	
			1	PLL_TX_EN = PLL_TX_EN_REG
			0	PLL_TX_EN = PLL_TX_EN_FSM

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8	0	BYPASS_VCO_RES	Bypass VCO tail resistor for max amplitude	
7	0	SDM_DITH_IN	SDM dither in value	
			1	Value 1
			0	Value 0
6	0	SDM_DITH_EN	SDM dither enable	
			1	Enable the SDM dither
			0	Disable the SDM dither
5	0	DAC_RANG_MN	Select the source of DAC_RANG	
			1	DAC_RANG = DAC_RANG_REG
			0	DAC_RANG = DAC_RANG_FSM
4	0	SYNC_DET_DIS	Disable AGC when sync detected	
3	0	AFC_EN_REG	AFC enable	
			1	Enable the AFC
			0	Disable the AFC
2	0	AFC_EN_MN	Select the source of AFC_EN	
			1	AFC_EN = AFC_EN_REG
			0	AFC_EN = AFC_EN_FSM
1	0	CTUNING_MN	Select the source of CTUNING	
			1	CTUNING = CTUNING_REG
			0	CTUNING = CTUNING_FSM
0	0	FTUNING_MN	Select the source of FTUNING	
			1	FTUNING = FTUNING_REG
			0	FTUNING = FTUNING_FSM

PLL_CTL1 (RW) Address: 02h

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
REG_TX_PA_WAIT							
8'h10							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Tx_PLL_WAIT							
8'h42							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REG_AFC_WAIT							
8'h00							
RW							

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Description of Word

Bit	Value	Symbol	Description
23:16	8'h10	REG_TX_PA_WAIT	The time between power up PA to transmit data
			8'hff 255 cycle
			...
			1 1 cycle
			0 0 cycle
15:8	8'h42	Tx_PLL_WAIT	PLL lock wait time in Tx mode
			8'hff 255 us
			...
			1 1 us
			0 0 us
7:0	8'h00	REG_AFC_WAIT	The time between RC done and AFC start
			8'hff 255 us
			...
			1 1 us
			0 0 us

CAL_CTL (RW) Address: 03h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Rx_pll_wait							
8'h28							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	afc_w_sel		Reserved	Bp_dc	Bp_dac	Bp_afc	Bp_rc
0	11		1	0	0	0	0
RW	RW		RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
bp_vco_ldo	Pseudo_rnd	Bp_rx_addr	bp_vco_amp	Bp_cp_diox	Vco_ldo_cal_reg		
0	0	0	0	1	0		
WR	RW	RW	RW	RW			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Vco_ldo_cal_mn	Rc_cal_ctr_mn	PLL_rst_cnt	Rc_cal_ctl_reg				
0	0	1	0				
RW	RW	RW	RW				

Description of Word

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Bit	Value	Symbol	Description
31:24	8'h28	Rx_pll_wait	PLL lock wait time in rx mode Force_cal : before every transmit and receive do calibration
23	0	Reserved	
22:21	11	afc_w_sel	Select the AFC wait reference counter
			0 512
			1 255
			2 127
			3 63
20	1	Reserved	
19	0	Bp_dc	Bypass DC calibration phase
			0 Disable
			1 Enable
18	0	Bp_dac	Bypass DAC calibration phase
			0 Disable
			1 Enable
17	0	Bp_afc	Bypass AFC calibration phase
			0 Disable
			1 Enable
16	0	Bp_rc	Bypass RC calibration phase
			0 Disable
			1 Enable
15	0	bp_vco_ldo	Bypass VCO_LDO calibration phase
			0 Disable
			1 Enable
14	0	Pseudo_rnd	Transmit Random data
			0 Disable
			1 Enable
13	0	Bp_rx_addr	Bypass the RX_ADDR phase in the main FSM
12	0	bp_vco_amp	Bypass VCO amplitude calibration phase
			0 Disable
			1 Enable
11	1	Bp_cp_diox	Bpassdio
			0 Disable
			1 Enable
10:8	0	Vco_ldo_cal_re g	Vco_ldomamual set value
7	0	Vco_ldo_cal_m n	Vcoldo calibration select
			0 Vco_ldo_cal = vco_ldo_cal_fsm
			1 Vco_ldo_cal = vco_ldo_cal_reg

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6	0	Rc_cal_ctr_mn	Rc calibration select	
			0	Rc_cal_ctr = rc_cal_ctr_fsm
			1	Rc_cal_ctr = rc_cal_ctr_reg
5	1	Pll_rst_cnt	Pll_rst_cnt	
			0	Output 0
			1	Output 1
4:0	0	Rc_cal_ctr_reg	Rc calibration register	

STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	SYNC_DS	CE	RX_P_NO		TX_FULL
0	0	0	0	0	2'b11		0
R	RW	RW	RW	R	R		R

Description of Word

Bit	Value	Symbol	Description	
7	0	BANK	Register BANK status	
			1	Register R/W is to register BANK1
			0	Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.	
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. Write 1 to clear bit.	
4	0	SYNC_DS	RX sync detector interrupt, Write 1 to clear bit. If SYNC_DS is asserted it must be cleared to enable further communication.	
3	0	CE	CE state	
2:1	2'b11	RX_P_NO	Data pipe number for the payload available for reading from RX_FIFO	
			11	RX FIFO Empty
			00-10	Data Pipe Number
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

STATE (RW) Address: 08h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				CAL_ST_CS			
0				0			
RW				R			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

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Reserved	STATE_CS
0	0
RW	R

Description of Word

Bit	Value	Symbol	Description
15:12	0	Reserved	
11:8	4'b0	Cal_st_cs	Describe the state of calibration state machine
7:6	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
5:0	6'b0	State_cs	Describe the state of main state machine

CHAN (RW) Address: 09h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Chan_mn	Reserved	CHAN_FRAC_REG					
0	0	0					
RW	RW	RW					
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CHAN_FRAC_REG							
0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CHAN_FRAC_REG							CHAN_INT_REG
0							0
RW							RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHAN_INT_REG							
0							
RW							

Description of Word

Bit	Value	Symbol	Description
31	1'b0	Chan_mn	Channel int and frac part select
			0 Come from the calculation from rf_ch

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			1	Come from register
30	2'b0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
29:9	0	CHAN_FRAC_REG	PLL frequency fragment pat	
8:0	0	CHAN_INT_REG	PLL frequency integer pat	

FDEV (RW) Address: 0ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	FDEV						
0	0x20						
R	RW						

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	
6:0	7'h20	FDEV	The max offset of the frequency

DAC_RANGE (RW) Address: 0dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DAC_RANGE_REG						
0	0						
R	RW						

Description of Word

Bit	Value	Symbol	Description
7:6	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
5:0	6'b0	DAC_RANGE_REG	DAC calibration Range control

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CTUNING (RW) Address: 0fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved			CTUNING_REG_RX				
0			0				
R			RW				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			CTUNING_REG_TX				
0			0				
R			RW				

Description of Word

Bit	Value	Symbol	Description
15:13	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
12:8	6'b0	CTUNING_REG_RX	AFC coarse tuning register control
7:5	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
4:0	6'b0	CTUNING_REG_TX	AFC coarse tuning register control

FTUNING (RW) Address: 10h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved					FTUNING_REG_RX		
0					0		
R					RW		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					FTUNING_REG_TX		
0					0		
R					RW		

Description of Word

Bit	Value	Symbol	Description
15:11	0	Reserved	Only 0 allowed

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			0	Keep the current value
			1	Reset to default values
10:8	3'b0	FTUNING_RE G_RX	AFC fine tuning register control	
7:3	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
2:0	3'b0	FTUNING_RE G_TX	AFC fine tuning register control	

RX_CTRL (RW) Address: 11h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
sbe_max_th			xcorr_th[6:2]				
0	0	1	1	0	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
xcorr_th[1:0]		en_dc_removal	en_sbe	reserved		h_idx	
0	0	1	1	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
15:13	3'b001	sbe_max_th	Sync address error tolerance
12:6	7'h50	xcorr_th	Sync threshold
5	1	en_dc_removal	Dc remove enable
4	1	en_sbe	Sbe enable
3:2	1	Reserved	
1:0	2'b10	h_idx	modulation index: when 1: 0.32, when 2: 0.50;

FAGC_CTRL_1 (RW) Address: 13h

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
reserved			pkdet_vrefc			pkdet_vref2c	
0			3'h2			1	
RW			RW			RW	

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Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
reserved	agc_dpd_lo_thr[10:4]						
0	7'h8						
RW	RW						
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
agc_dpd_lo_thr[3:0]				Reserved			VCO_AMP_MN
4'h1				0			0
RW				RW			RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO_AMP_CTL				VCO_PKREF_CTL			
4'h0				4'h3			
RW				RW			

Description of Word

Bit	Value	Symbol	Description
31:29	0	reserved	
28:26	3'b010	pkdet_vrefc	Pkdetvrefc value
25:24	2'b01	pkdet_vref2c	Pkdet vref2c value
23	0	reserved	
22:12	11'h081	agc_dpd_lo_thr	Agc_dpd_lo threshold
11:9	0	reserved	
8	0	VCO_AMP_MN	Manual mode of VCO amplitude calibration
7:4	4'h0	VCO_AMP_CTL	VCO amplitude control
3:0	4'h3	VCO_PKREF_CTL	VCO amplitude calibration reference

DOC_DACI (RW) Address: 1ah

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	doc_daci						
0	0						
RW	RW						

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	Only 0 allowed

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			0	Keep the current value
			1	Reset to default values
6:0	0	doc_daci	Doc calibration daci value	

DOC_DACQ (RW) Address: 1bh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	doc_dacq						
0	0						
RW	RW						

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
6:0	0	doc_dacq	Doc calibration dacq value	

AGC_CTRL (RW) Address: 1ch

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
test_pat_en	adp_samp_mode			agc_samp_mode		agc_dpd_mode	agc_dpd_thr_db[5]
0	0	0	0	1	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
agc_dpd_thr_db[4:0]				agc_dpd_thr[10:8]			
1	0	0	1	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
agc_dpd_thr[7:0]							
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
23	0	test_pat_en	Test pattern enable

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22:20	0	adp_samp_mode	Number of clock cycles delay between every two apd detection: When 0, 0 cycles When 1, 2 cycles When 2, 4 cycles When 3, 8 cycles When 4, 16 cycles When 5, 32 cycles
19:18	2	agc_samp_mode	The number of shift registers which are required for Dpd calculation. When 0, 2 registers When 1, 4 registers When 2, 8 registers When 3, 16 registers
17	0	agc_dpd_mode	'0': mean of sample amplitudes, '1': max of sample amplitudes;
16:11	33	agc_dpd_thr_db	dB value of dpd_hi_th minus back off dB value of the Dpd which is 3 in default.
10:0	200	agc_dpd_thr	Default threshold when dpd is detected.

AGC_GAIN (RW) Address: 1dh

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
agc_gain_mn	apd_clr_cnt_th					apd_det_cnt_th[4:3]	
0	0	0	1	1	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
apd_det_cnt_th[2:0]			dpd_clr_cnt_th[5:1]				
1	1	1	0	1	0	1	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
dpd_clr_cnt_th[0]	reserved		Agc_apd_state_reg[1:0]		Agc_dpd_state_reg[2:0]		
1	1	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Agc_dpd_state_reg[10:3]							
0	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
31	0	agc_gain_mn	Agc output gain is get from software or hardware calculation
			1 From software

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			0	From hardware
30:26	7	apd_clr_cnt_th [4:0]	Analog Gsw+Gsetl time interval	
25:21	7	apd_det_cnt_th [4:0]	Apd detection time interval	
20:15	6'h17	dpd_clr_cnt_th [5:0]	Digital Gsw+Gsetl time interval, and add Dpd detection time interval	
14:13	2	reserved		
12:11	0	Agc_apd_state_r eg	When agc_gain_mn is 1, the value read from this register is the Lna gain given by the software. When agc_gain_mn is 0, the value read from this register is the Lna gain calculated from the hardware module	
10:0	101	Agc_dpd_state_ reg	When agc_gain_mn is 1, the value read from this register is the filter gain given by the software. When agc_gain_mn is 0, the value read from this register is the filter gain calculated from the hardware module	

RF_IVGEN (RW) Address: 1eh

Bit23	Bit 22	Bit 21	Bit 20	Bit19	Bit 18	Bit 17	Bit16
Calib_rx_reg	Tx_0_1_rvs	Pd_lna_reg	Pd_lna_mn	Pd_pa_reg	Pd_pa_mn	Tia_lobias	
1	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit13	Bit12	Bit 11	Bit 10	Bit 9	Bit 8
Pd_adc_ldo_re g	Pd_adc_ldo_m n	Pd_mix_reg	Pd_mix_mn	Bm_filter[1:0]		Bm_lna	
0	0	0	0	01		00	
RW	RW	RW	RW	RW		RW	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pa_voltage	Pd_xtal_reg	Pd_xtal_mn	Xtal_cc				
0	0	0	1	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
23	1	Calib_rx_reg	Manual calibration TX/RX select
			1 Manual calibration for RX
			0 Manual calibration for TX
22	0	Tx_0_1_rvs	TX 0/1 reverse
			1 Reverse the 0/1 when transmit
			0 Not reverse
21	0	Pd_lna_reg	Pd_lna manual value

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20	0	Pd_lna_mn	Pd_lna manual select	
			1	from register
			0	From FSM
19	0	Pd_pa_reg	Pd_pa manual value	
18	0	Pd_pa_mn	Pd_pa manual select	
			1	from register
			0	From FSM
17:16	1	Tia_lobias	Output to analogue	
15	0	Pd_adc_ldo_reg	Pd_adc_ldo manual value	
14	0	Pd_adc_ldo_mn	Pd_adc_ldo manual select	
			1	from register
			0	From FSM
13	0	Pd_mix_reg	Pd_mix manual value	
12	0	Pd_mix_mn	Pd_mix manual select	
			1	from register
			0	From FSM
11:10	2'b01	Bm_filter	Filter bias current control	
9:8	2'b00	Bm_lna	Output to analogue	
7	0	Pa_voltage	Pa voltage output to analogue	
6	0	Pd_xtal_reg	Pd_xtal manual value	
5	0	Pd_xtal_mn	Pd_xtal manual select	
4:0	5'b11111	Xtal_cc	Output to analogue	

TEST_PKDET (RW) Address: 1fh

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
test_en	Reserved			miso_drv		pll_icp_sel	
0	0			0	1	0	1
RW	RW			RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
test_mode			test_point_sel1			test_point_sel0	
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
xtal_resc		bm_xtal	Reserved	pll_vdiv2_sel		pd_vco_pkdet_mn	pd_vco_pkdet_reg
0	0	1	0	1	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

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Bit	Value	Symbol	Description
23	0	test_en	Test mode enable
22:20	0	reserved	
19:18	2'b01	miso_drv	Output driving capability of MISO
17:16	2'b01	pll_icp_sel	Charge pump current control
15:14	3'b000	test_mode	Test mode select
12:10	3'b000	test_point_sel1	Test point select
9:8	2'b00	test_point_sel0	Test point select
7:6	2'b00	xtal_resc	Resistor value control of xtal bias
5	1	bm_xtal	Xtal bias current control
4	0	Reserved	
3:2	2'b11	pll_vdiv2_sel	Div2 dc bias control, pll_vdiv2_sel should be set 01 for normal work
1	0	pd_vco_pkdet_mn	Manual mode enable of pd_vco_pkdet
0	0	pd_vco_pkdet_reg	Manual mode register of pd_vco_pkdet